# COEP Technological University, Pune

**(A Unitary Public University of Govt. of Maharashtra)**

## NEP 2020 Compliant

Curriculum Structure

## M. Tech
## VLSI Design

**(Effective from: A.Y. 2026-27)**

## Program Outcomes (POs)

1. **PO1: (Core Technical Competence):** Ability to apply advanced knowledge of Graph Theory, IC fabrication, RTL simulation, and analog/digital design to solve complex VLSI engineering problems.
2. **PO2: (Modern Tool Usage & Synthesis):** Proficiency in using industry-standard EDA tools (e.g., Cadence, Xilinx, Mentor Graphics) for the synthesis, physical design, and verification of System-on-Chip (SoC) architectures.
3. **PO3: (Research & Communication Excellence):** Capacity to conduct independent research, demonstrate ethical practices, and communicate technical findings effectively through industry-standard documentation and presentations.

# Curriculum Structure for M. Tech – VLSI Design

## Semester I

| Sr. No. | Course Type | Course Code | Course Name | L | T | P | S | Cr | Evaluation Scheme (Weightages in %) | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | Theory | | | Laboratory | |
| | | | | | | | | | MSE | TA | ESE | ISE | ESE |
| 1. | PSMC | EVD-25001 | Graph, Field and Ring Theory for Security and Physical design | 3 | 1 | - | 1 | 4 | 30 | 20 | 50 | - | - |
| 2. | PSBC | EVD-25004 | IC Fabrication Techniques | 2 | 1 | - | 1 | 3 | 30 | 20 | 50 | - | - |
| 3. | **PCC** | EVD-25002 | RTL Simulation and Synthesis | **3** | - | **2** | **1** | **4** | **30** | **20** | **50** | **50** | **50** |
| 4. | **PCC** | EVD-25003 | Digital IC Design | **3** | **-** | **2** | **1** | **4** | **30** | **20** | **50** | **50** | **50** |
| 5. | **PCC** | EVD-25005 | Analog IC Design | **3** | **-** | **2** | **1** | **4** | **30** | **20** | **50** | **50** | **50** |
| 6. | PEC-1 | EVD (PE) | Program Specific Elective –I<br>a) Next generation computer Architectures<br>b) Machine Learning<br>c) SoC architecture | 3 | - | - | 1 | 3 | 30 | 20 | 50 | - | - |
| 7. | AEC | SET-25002 | Technical Communication Skills | 1 | - | 2 | 1 | 2 | 50 | 50 | - | 100 | |
| **Total Credits** | | | | | | | | **24** | | | | | |

# Curriculum Structure for M. Tech – VLSI Design

## Semester II

| Sr. No. | Course Type | Course Code | Course Name | L | T | P | S | Cr | Evaluation Scheme (Weightages in %) | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | Theory | | | Laboratory | |
| | | | | | | | | | MSE | TA | ESE | ISE | ESE |
| 1. | OE | OEC | Open Elective - Networked Embedded System Design (to be offered to other dept) | 3 | - | - | 1 | 3 | 30 | 20 | 50 | - | - |
| 2. | PCC | EVD-25006 | Verification using SV and UVM | **3** | **-** | **2** | **1** | **4** | **30** | **20** | **50** | **50** | **50** |
| 3. | PCC | EVD-25007 | VLSI Physical Design | **3** | **-** | **2** | **1** | **4** | **30** | **20** | **50** | **50** | **50** |
| 4. | PCC | EVD-25008 | RF Circuit Design | **3** | **-** | **2** | **1** | **4** | **30** | **20** | **50** | **50** | **50** |
| 5. | PEC-2 | EVD(PE) | Program Specific Elective –II<br>a) VLSI Testing<br>b) VLSI architectures for Signal Processing<br>c) Hardware / Software Co-design<br>d) Mixed Signal Circuit Design | 3 | - | - | 1 | 3 | 30 | 20 | 50 | - | - |
| 6. | PEC-3 | EVD(PE) | Program Specific Elective –III<br>a) Advanced VLSI Design<br>b) Nano-electronic material and devices<br>c) Hardware Security<br>d) Device Modelling | 3 | - | - | 1 | 3 | 30 | 20 | 50 | - | - |
| 7. | RM | SET-25001 | Research Methodology | 2 | 1 | - | 1 | 3 | 30 | 20 | 50 | - | - |
| 8. | LLC | LL-250XX | Liberal Learning Course | - | - | 2 | 2 | 1 | - | - | - | 100 | - |
| **Total Credits** | | | | | | | | **25** | | | | | |

# Curriculum Structure for M. Tech – VLSI Design

## Semester III

| Sr. No. | Course Type | Course Code | Course Name | L | T | P | S | Cr | Evaluation Scheme (Weightages in %) | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | Theory | | | Laboratory | |
| | | | | | | | | | MSE | TA | ESE | ISE | ESE |
| 1 | SLC | EVD (OC) 250XX | Massive Open Online Course –I | 3 | - | - | 1 | 3 | - | - | 100 | - | - |
| 2 | SLC | EVD (OC) 250XX | Massive Open Online Course –II | 3 | - | - | 1 | 3 | - | - | 100 | - | - |
| 3 | OJT | <tbd> | Internship | - | - | - | - | 3 | - | - | 100 | - | - |
| 4 | Project | EVD 25009 | Dissertation Phase – I | - | - | 22 | 12 | 11 | - | - | - | 30 | 70 |
| **Total Credits** | | | | **20** | | | | | | | | | |

## Semester IV

| Sr. No. | Course Type | Course Code | Course Name | L | T | P | S | Cr | Evaluation Scheme (Weightages in %) | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | Theory | | | Laboratory | |
| | | | | | | | | | MSE | TA | ESE | ISE | ESE |
| 1 | Project | EVD 25010 | Dissertation Phase – II | - | - | 22 | 12 | 11 | - | - | - | 30 | 70 |
| **Total Credits** | | | | **11** | | | | | | | | | |

- **MOOC Courses Identified:**
  - Real Time Embedded Systems
  - VLSI design for Fault Tolerance and Testability
  - Parallel Computing
  - Advanced IOT Applications