COEP Technological University, Pune

(A Unitary Public University of Govt. of Maharashtra)

NEP 2020 Compliant

Curriculum Structure

M. Tech
VLSI Design

(Effective from: A.Y. 2025-26)

Program Outcomes (POs)

1. **PO1: (Core Technical Competence):** Ability to apply advanced knowledge of Graph Theory, IC fabrication, RTL simulation, and analog/digital design to solve complex VLSI engineering problems.
2. **PO2: (Modern Tool Usage & Synthesis):** Proficiency in using industry-standard EDA tools (e.g., Cadence, Xilinx, Mentor Graphics) for the synthesis, physical design, and verification of System-on-Chip (SoC) architectures.
3. **PO3: (Research & Communication Excellence):** Capacity to conduct independent research, demonstrate ethical practices, and communicate technical findings effectively through industry-standard documentation and presentations.

Curriculum Structure for M. Tech – VLSI Design

Semester I

Sr. No.	Course Type	Course Code	Course Name	L	T	P	S	Cr	Evaluation Scheme (Weightages in %)				
									Theory			Laboratory	
									MSE	TA	ESE	ISE	ESE
1.	PSMC	EVD-25001	Graph, Field and Ring Theory for Security and Physical design	3	1	-	1	4	30	20	50	-	-
2.	PSBC	EVD-25004	IC Fabrication Techniques	2	1	-	1	3	30	20	50	-	-
3.	**PCC**	EVD-25002	RTL Simulation and Synthesis	**3**	-	**2**	**1**	**4**	**30**	**20**	**50**	**50**	**50**
4.	**PCC**	EVD-25003	Digital IC Design	**3**	**-**	**2**	**1**	**4**	**30**	**20**	**50**	**50**	**50**
5.	**PCC**	EVD-25005	Analog IC Design	**3**	**-**	**2**	**1**	**4**	**30**	**20**	**50**	**50**	**50**
6.	PEC-1	EVD (PE)	Program Specific Elective –I a) Next generation computer Architectures b) Machine Learning c) SoC architecture	3	-	-	1	3	30	20	50	-	-
7.	RM	SET-25001	Research Methodology	2	1	-	1	3	30	20	50	-	-
			Total Credits					**25**					

Curriculum Structure for M. Tech – VLSI Design

Semester II

Sr. No.	Course Type	Course Code	Course Name	L	T	P	S	Cr	Evaluation Scheme (Weightages in %)				
									Theory			Laboratory	
									MSE	TA	ESE	ISE	ESE
1.	OE	OEC	Open Elective - Networked Embedded System Design (to be offered to other dept)	3	-	-	1	3	30	20	50	-	-
2.	PCC	EVD-25006	Verification using SV and UVM	**3**	**-**	**2**	**1**	**4**	**30**	**20**	**50**	**50**	**50**
3.	PCC	EVD-25007	VLSI Physical Design	**3**	**-**	**2**	**1**	**4**	**30**	**20**	**50**	**50**	**50**
4.	PCC	EVD-25008	RF Circuit Design	**3**	**-**	**2**	**1**	**4**	**30**	**20**	**50**	**50**	**50**
5.	PEC-2	EVD(PE)	Program Specific Elective –II a) VLSI Testing b) VLSI architectures for Signal Processing c) Hardware / Software Co-design d) Mixed Signal Circuit Design	3	-	-	1	3	30	20	50	-	-
6.	PEC-3	EVD(PE)	Program Specific Elective –III a) Advanced VLSI Design b) Nano-electronic material and devices c) Hardware Security d) Device Modelling	3	-	-	1	3	30	20	50	-	-
7.	AEC	SET-25002	Technical Communication Skills	1	-	2	1	2	50	50	-	100	
8.	LLC	LL-250XX	Liberal Learning Course	-	-	2	2	1	-	-	-	100	-
			Total Credits					**24**					

Curriculum Structure for M. Tech – VLSI Design

Semester III

Sr. No.	Course Type	Course Code	Course Name	L	T	P	S	Cr	Evaluation Scheme (Weightages in %)				
									Theory			Laboratory	
									MSE	TA	ESE	ISE	ESE
1	SLC	EVD (OC) 250XX	Massive Open Online Course –I	3	-	-	1	3	-	-	100	-	-
2	SLC	EVD (OC) 250XX	Massive Open Online Course –II	3	-	-	1	3	-	-	100	-	-
3	OJT	<tbd>	Internship	-	-	-	-	3	-	-	100	-	-
4	Project	EVD 25009	Dissertation Phase – I	-	-	22	12	11	-	-	-	30	70
Total Credits								**20**					

Semester IV

Sr. No.	Course Type	Course Code	Course Name	L	T	P	S	Cr	Evaluation Scheme (Weightages in %)				
									Theory			Laboratory	
									MSE	TA	ESE	ISE	ESE
1	Project	EVD 25010	Dissertation Phase – II	-	-	22	12	11	-	-	-	30	70
Total Credits								**11**					

- **MOOC Courses Identified:**
  - Real Time Embedded Systems
  - VLSI design for Fault Tolerance and Testability
  - Parallel Computing
  - Advanced IOT Applications

Graph, Field and Ring Theory for Security and Physical design						
Course Code	EVD-25001		**Examination Scheme**			
Teaching Scheme	3-1-0-1		**Theory**	TA: 20	MSE: 30	ESE: 50
Credits	4		**Laboratory**			--

Course Outcomes: Students will be able to:

1. Understand the various types of graphs, graph properties and give examples for the given property
2. Model the given problem from their field to underlying graph model.
3. Proceed to solve the problem either through approximation algorithm or exact algorithm depending on the problem nature.
4. Appreciate the applications of digraphs and graphs in various communication networks.
5. Appreciate the applications of graphs and digraphs in various other fields.

Directed graphs: **[6 Hrs]**

some standard definitions and examples of strongly, weakly, unilaterally connected digraphs, strong components and deadlock. Matrix representation of graph and digraphs. Some properties (proof not expected). Eulerian graphs and standard results relating to characterization of Eulerian graphs. Hamiltonian graph-standard theorems (Dirac theorem, Chavtal theorem, closure of graph). Non-Hamiltonian graph with maximum number of edges.
Self-centered graphs and related simple theorems.

Chromatic number: **[6 Hrs]**

vertex chromatic number of a graph, edge chromatic number of a graph (only properties and examples)-application to colouring. Planar graphs, Euler's formula, maximum number of edges in a planar graph, some problems related to planarity and non-planarity, five colour theorem, Vertex Covering, Edge Covering, Vertex independence number, Edge independence number, relation between them and number of vertices of a graph.

Matching Theory and Directed Structures **[6 Hrs]**

Matching theory, maximal matching and algorithms for maximal matching. Perfect matching (only properties and applications to regular graphs). Tournaments, some simple properties and theorems on strongly connected tournaments. Application of Eulerian digraphs.

Graph Algorithms **[6 Hrs]**

DFS-BFS algorithm, shortest path algorithm, Min-spanning tree and Max-spanning tree algorithm, Planarity algorithm. Flows in graphs; Maxflow mincut theorem, algorithm for maxflow. PERT-CPM. Complexity of algorithms; P-NP-NPC-NP hard problems and examples.

Network Flows and Complexity **[6 Hrs]**

Flows in graphs, Max-flow Min-cut theorem, algorithms for maximum flow. PERT-CPM techniques. Complexity of algorithms: P, NP, NP-Complete, NP-Hard problems with examples.

Self-Study (SS): **[6 Hrs]**

Advanced graph concepts such as graph isomorphism and graph minors. Introduction to real-world applications including social networks and communication systems.
Overview of approximation techniques for NP-hard graph problems. Case studies highlighting the use of graph algorithms in engineering and computer science.

Textbooks:

[1] J.A. Bondy and U.S.R. Murthy, *Graph Theory with Applications*, Macmillan, London, 1976.

[2] Cormen, Leiserson, Rivest and Stein, *Introduction to Algorithms*, 2nd Edition, McGraw-Hill, 2001.

Reference Books:	
[1]	M. Gondran and M. Minoux, *Graphs and Algorithms*, John Wiley, 1984.
[2]	H. Gerez, *Algorithms for VLSI Design Automation*, John Wiley, 1999.
Note:	
[1] [2] [3] [4] [5]	To measure CO1, questions may be of the type: define, identify, list, and explain graph properties To measure CO2, questions may be based on modelling real-world problems using graphs. To measure CO3, questions may involve solving algorithmic problems using graph techniques. To measure CO4, questions may focus on applications in networks and systems. To measure CO5, questions may include interdisciplinary applications and case studies

IC Fabrication Techniques						
Course Code	EVD-25004		**Examination Scheme**			
Teaching Scheme	2-1--0-1		**Theory**	TA: 20	MSE: 30	ESE: 50
Credits	3		**Laboratory**			--
Course Outcomes: Students will be able to:						
1. Analyze Semiconductor Material Processing and Cleanroom Standards 2. Evaluate and Model Unit Fabrication Processes 3. Synthesize Complete Process Flows and TCAD Simulations						

Crystal Growth and Wafer Preparation	**[6 Hrs]**
Semiconductor materials: Silicon, Germanium, and compound semiconductors. Crystal growth techniques: Czochralski (CZ) and Float Zone (FZ), doping in melt. Wafering processes including slicing, lapping, polishing, and cleaning (RCA process). Cleanroom technology: airborne particulate classification, laminar flow, and safety practices.	
Lithography and Etching	**[6 Hrs]**
Photolithography: photoresists (positive and negative), mask generation, exposure systems (stepper/scanner). Advanced lithography: electron-beam, X-ray, and ion-beam techniques. Etching processes: wet chemical etching and dry etching methods such as plasma and reactive ion etching (RIE), selectivity considerations.	
Thin Film Deposition and Oxidation	**[6 Hrs]**
Oxidation: kinetics of thermal oxidation using Deal-Grove model, dry and wet oxidation. Chemical Vapor Deposition (CVD): APCVD, LPCVD, PECVD. Physical Vapor Deposition (PVD): thermal evaporation, electron-beam evaporation, sputtering.	
Diffusion and Ion Implantation	**[6 Hrs]**
Diffusion: Fick's laws, constant source and limited source diffusion, drive-in oxidation. Ion implantation: range theory, projected range, straggle, channelling effects. Annealing: rapid thermal annealing (RTA) and lattice damage recovery.	
Metallization and Process Integration	
Metallization: ohmic and Schottky contacts, multilevel interconnects, electromigration. Process integration: isolation techniques such as LOCOS and shallow trench isolation, CMP (Chemical Mechanical Polishing). Device fabrication flow: CMOS, BiCMOS, NMOS, PMOS, and advanced devices including GaN-based devices.	

Self-Study (SS):	**[6 Hrs]**
Process simulation of ion implantation, diffusion, oxidation, epitaxy, lithography, etching, and deposition using TCAD tools. Introduction to modern fabrication challenges and emerging semiconductor technologies.	

Textbooks:

[1]	Marc J. Madou, *Fundamentals of Microfabrication and Nanotechnology*, CRC Press.
[2]	Richard C. Jaeger, *Introduction to Microelectronic Fabrication*, Prentice Hall.

Reference Books:

[1]	S. M. Sze, *Semiconductor Devices: Physics and Technology*, Wiley
[2]	Plummer, Deal, Griffin, *Silicon VLSI Technology*, Pearson
[3]	Jaeger, *Introduction to Microelectronic Fabrication*, Prentice Hall

Note:

[1]	To measure CO1, questions may be of the type: explain, describe, and analyze fabrication processes.
[2]	To measure CO2, questions may involve modeling and evaluation of fabrication techniques.
[3]	To measure CO3, questions may include synthesis of process flows and simulation-based problems.
[4]	To measure SS, questions may be based on TCAD simulations and emerging fabrication technologies.

RTL Simulation and Synthesis

Course Code	EVD-25002		**Examination Scheme**			
Teaching Scheme	3-0-2-1		**Theory**	TA: 20	MSE: 30	ESE: 50
Credits	3		**Laboratory**	ISE:50	ESE:5	

Course Outcomes: Students will be able to:

1. Understand and explain the concepts of **Register Transfer Level (RTL) design**, abstraction levels, and their role in the VLSI design flow
2. Design and implement **combinational and sequential digital circuits** using HDLs such as Verilog / SystemVerilog
3. Develop and analyze **Finite State Machines (FSMs)** and control logic for digital systems using appropriate state encoding and RTL coding styles.
4. Analyze different types of timing paths for setup and hold conditions.
5. Design and integrate **datapath and control path architectures** for medium-complexity digital systems such as ALUs, FIFOs, and simple processors
6. Analyze various **instruction formats, addressing modes, and instruction types**, and evaluate their impact on performance and complexity

HDL and Digital Building Blocks:	**[10 Hrs]**
Hardware Description Language: HDL Fundamentals and Design entry by Verilog / System Verilog, Test benches.Digital Building Blocks: Combinatorial and Sequential building blocks using System Verilog **Simulation region:** System tasks, Active Events, Inactive Events, Non-blocking Events, and Monitor Events for System Verilog.	

Sequential Logic Design	**[12 Hrs]**
Top-down approach to Design, Synchronous FSM design (Mealy and Moore Machines), **STA** -Static Timing analysis, Meta-stability, Propagation delay, Contamination delay, Set up and hold time , slack calculation, clock issues, Rise Time, Fall time, delay modeling, Clock domain crossing Asynchronous FSM Design IP in various forms: Soft IP, Hard IP, case studies. Configurable Logic Devices: Fused and anti fused technologies, PAL, PLA, FPGA implementation.	
Data Path and Control Path Design:	**[6 Hrs]**
Unsigned multiplication, Signed multiplication, GCD computation.	
Instruction set Architecture	[6 Hrs]
Types of ISA, ISA vs Micro architecture, MIPS ISA, instructions encoding, MIPS general purpose registers, signed unsigned instructions, floating point instructions, Pseudo instructions, Multiport register File, Memory modeling	
HDL representation for MIPS architecture	**[6 Hrs]**
Addressing modes, Exceptions, HDL representation of single cycle CPU data path and control path. Control path and Data path design of Multi cycle Processor and a Pipe-lined processor, Performance analysis.	
Self-Study (SS):	**[6 Hrs]**
Custom ISA design for specific applications, Super scalar and out of order execution, sIMD/ vector architecture	

Textbooks:

[1]	Stephen Brown and ZvonkoVranesic, “Fundamentals of Digital logic with Verilog Design”, Mc-GrawHill, 3rd edition
[2]	David Harris and Sarah Harris, “Digital Design and Computer Architecture”, Morgan Kaufmann.

Reference Books:

[1]	Doug Amos, Austin Lesea, Rene Richter, “FPGA based prototyping methodology manual”, Xilinx
[2]	Douglas Smith, “HDL Chip Design: A Practical Guide for Designing, Synthesizing & Simulating ASICs & FPGAs Using VHDL or Verilog”, Doone Publications.
[3]	Donald D Givone, “Digital principles and Design”, Tata Mc-Graw Hill
[4]	Janick Bergeron, “ Writing test benches, Functional verification of HDL modules” Kluwer Academic Publishers
[5]	Stuart Sutherland Simon Davidmann Peter Flake, “SystemVerilog For Design Second Edition”, Springer
[6]	IEEE standard HDL based on Verilog HDL, published by IEEE.

Note:

[1]	To measure CO1, questions may be of the type- define, identify, state, match, list, name etc.
[2]	To measure CO2, questions may be of the type- explain, describe, illustrate, evaluate, give examples, compute etc.
[3]	To measure CO3, questions will be based on applications of core concepts.
[4]	To measure CO4, questions may be of the type- true/false with justification, theoretical fill in the blanks, theoretical problems, prove implications or corollaries of theorems, etc.
[5]	To measure CO5, some questions may be based on self-study topics and comprehension of unseen passages.

RTL Simulation and Synthesis Lab						
Course Code	EVD-25002		**Examination Scheme**			
Teaching Scheme	3-0-2-1		**Theory**	TA: 20	MSE: 30	ESE: 50
Credits	4		**Laboratory**	ISE:50	ESE:5	

Course Outcomes: Students will be able to:

1. 1. Understanding the programmable and reprogrammable systems.
2. 2. Identify, formulate, solve and implement problems in signal processing, communication systems etc using RTL design tools.
3. 3. Use EDA tools like Xilinx, Quartus II and Mentor Graphics and Cadence

Journal Submission is in the form of CD. It should contain HDL codes, snapshot of results, synthesis reports, RTL view. In case the programs are downloaded on FPGA / SoC, the pre & post synthesis and implementation reports should also be submitted

List of Experiments

EDA tools: Xilinx / Quartus II and Mentor Graphics

Verilog implementation of –

1. EDA tools : Xilinx / Quartus II and Mentor Graphics and Cadence
2. Verilog implementation of 1. Mux/De-mux, Full Adder, 8-bit magnitude comparator, encoder/ decoder, priority encoder, D FF, 4 bit Shift registers (SISO, SIPO, PISO, bidirectional), Synchronous Counters, binary to gray converter, parity generator.
3. Sequence generator / detectors, Synchronous FSM – Mealy and Moore machines. 3. Vending machines - Traffic Light controller, ATM, elevator control.
4. Interfacing with peripherals like seven segment display, LED, UART, Custom GPIO, Temp sensor, Ethernet DDR.
5. SPI, I2C, PCI protocols, Bus Arbiter, UART
6. Image processing algorithms such as filtering, compression, Image enhancement resizing of Image etc
7. Single port SRAM, Synchronous and Asynchronous FIFO
8. MIPS (Microprocessor without interlock pipeline stages) design
9. Lab based on physical design (STA)

Digital IC Design						
Course Code	EVD-25003		**Examination Scheme**			
Teaching Scheme	3-0-2-1		**Theory**	TA: 20	MSE: 30	ESE: 50
Credits	4		**Laboratory**	CIE: 50	ESE: 50	--

Course Outcomes: Students will be able to:

1. Illustrate / Infer / Interpret the importance of manufacturing process of CMOS based integrated circuits, energy band diagrams of MOS, scaling technology and the secondary effect in MOSFETs.
2. Model MOS transistors, its small geometry effects and interconnect wire for performance analysis and Evaluate impact of technology scaling on Robustness, performance, and energy/power dissipation of CMOS Inverter.
3. Design / formulate / estimate simple and complex combinatorial logic circuit for optimized area, speed, power, glitch free and reduced supply voltages.
4. Design and analyse CMOS sequential circuits by applying bi-stability principles and conducting Static Timing Analysis (STA) to ensure robust data storage and timing closure against setup and hold constraints.
5. Design and optimize high-density SRAM systems by evaluating the trade-offs between 6T, 8T, and 10T cell topologies and integrating row and column peripheral circuitry to achieve balanced read/write stability, power efficiency, and area scaling.
6. Evaluate and classify the fundamental types of semiconductor memory by analysing their architectural differences, volatility, and performance metrics (speed, density, and cost) to select appropriate storage solutions for VLSI systems.

Introduction to VLSI: **[8 Hrs]**

Evolution of VLSI, Energy band diagram of MOS Capacitor, Operation and working of MOS Transistor, Derivation of Threshold voltage equation.

Technology Scaling and Road map, Scaling issues, Secondary effects in MOSFETS, Standard 4 mask NMOS Fabrication process, High–k dielectric, Metal Gate Technology, FinFET, IC layout design and tools: CMOS n-well process design rules, stick diagram, ASIC Design Flow.

Electrical wire models and CMOS Inverter: **[6 Hrs]**

MOS capacitances, Modelling of MOS transistors using SPICE level I and II equations, BSIM Models. The ideal wire, the lumped RC model, the distributed RC model, Elmore delay model.

Quality metrics of digital design: Cost, Functionality, Robustness, Power, and Delay. CMOS inverter: Switching Threshold, Noise Margin, Dynamic behavior of CMOS inverter, propagation delay of Inverter, RC Delay, Dynamic and Static Power consumption and Low power design criteria.

Combinational logic: **[8 Hrs]**

Static CMOS design, pass transistor logic, transmission gate logic, Logic effort delay, standard cell design, sizing of gates, estimating and optimizing delay in standard cell and clock distribution networks, Dynamic logic, Speed and power dissipation in dynamic logic, cascading dynamic gates.	
Sequential logic:	**[4 Hrs]**
Timing Constraints in CMOS latches and registers, Bi-stability principle, MUX based latches, Static SR flip-flops, Master slave edge-triggered register, Dynamic latches and registers, STA and max and min delay constraints for Flip-flop	
Array Subsystems:	**[3 Hrs]**
6T/8T/10T SRAM Cell design, Row Circuitry, Column circuitry, SRAM Cell Array design discussions from technical papers.	
Introduction to Storage devices for In-Memory Computation:	**[4 Hrs]**
Mass Data Storage devices and technology, Flash Memory, fundamental operating physics, Read/Write Mechanisms and performance metrics comparison in terms of unlimited write endurance, high-speed switching, and resistance to radiation for emerging memory devices like ferroelectric RAM, magneto resistive RAM, resistive Random Access Memory (RRAM), phase change material (PCM), nano magnetic and spintronic devices, Superconducting electronic memory for Quantum Information Processing (QIP).	

Textbooks:

[1]	N. Weste and D. Harris, “CMOS VLSI Design A Circuits and Systems Perspective”, 4th edition, Pearson.
[2]	J M Rabaey, A. Chandrakasan, B. Nikolic, “Digital Integrated Circuits A Design Perspective”, Pearson.

Reference Books:

[1]	Sung Mo Kang, Yusuf Leblebici, “CMOS digital integrated circuits”, TataMcGraw Hill Publication.
[2]	Baker Li Boyce, “CMOS Circuit Design, Layout, and Simulation”, Wiley, 2nd Edition.
[3]	Neil E Weste and Kamran Eshraghian, “Principle of CMOS VLSI Design”, Pearson education

Note:

[1]	To measure CO1, questions may be of the type- illustrate, interpret, infer, describe, calculate etc.
[2]	To measure CO2, questions may be of the type- explain, describe, illustrate, evaluate, give examples, compute etc.
[3]	To measure CO3, questions may be based on design, formulate, estimate etc.
[4]	To measure CO4, questions may be of the type- design and analyse, etc.
[5]	To measure CO5, some questions may be of type design, optimize and integrate etc.
[6]	To measure CO6, some questions may be of type evaluate, analyse, classify etc.

Digital IC Design Lab			
Laboratory	ISE: 50	ESE: 50	
Course Outcomes: Students will be able to:			
1. Interpret the behaviour of MOS Transistor with the help of SPICE tools. 2. DC and Transient analysis of CMOS Inverter. 3. Physical design and Verification of CMOS Inverter. 4. Design of digital circuits, clock and buffer distribution networks for standard cell design according to design specs provided.			
List of Practical			
1. DC analysis of NMOS and PMOS Transistor using NGSPICE. Estimate I_{ON}, I_{OFF}, S and λ for 180nm / 130nm / 90nm channel length transistors. 2. V_{th} analysis of NMOS and PMOS Transistor using various methods. 3. DC and Transient analysis of CMOS Inverter using NGSPICE. Estimate V_{IL}, V_{IH}, V_{OL}, V_{OH}, NM_L, NM_H from DC analysis and tp_{HL}, tp_{LH} from transient analysis. 4. Design of 5 stage and 7 stage ring oscillators using NGSPICE. Estimate f_{osc}. 5. Schematic design of CMOS Inverter and its DC, Transient analysis using Cadence EDA Tool. 6. Schematic to Symbol generation using Cadence EDA Tool. 7. Schematic to Layout of CMOS Inverter using Cadence EDA Tool. 8. Post Layout simulation of CMOS Inverter and Parasitic Extraction. 9. Design of all basic gates and /or combinatorial circuits using Cadence EDA Tool. 10. Design of a 6 Transistor SRAM cell using Cadence EDA Tool. Estimate CR and PR, Read SNM and Write SNM. 11. Design of Sequential circuits like D FF, simple clock and buffer distribution networks for standard cell design using Cadence EDA Tool.			

Analog IC Design						
Course Code	EVD-25005		**Examination Scheme**			
Teaching Scheme	3-0-2-1		**Theory**	TA: 20	MSE: 30	ESE: 50
Credits	4		**Laboratory**			--
Course Outcomes: Students will be able to:						
1. Interpret the graphical techniques for modelling Analog circuits and MOS transistor small geometry effects. 2. Design / formulate / estimate Analog sub circuits and cascaded stages for current and voltage gain, input and output impedances and frequency response. 3. Articulate the knowledge of analog sub circuits to design OP AMPS						
Foundation:						**[6 Hrs]**
Analog Landscape, Techniques for intuitive and graphical understanding of analog circuits viz R, L, C and dependent V and I sources and their combinations, Large Signal and Small Signal Models of MOS Transistors.						
Analog Sub-circuits:						**[6 Hrs]**
Stability, Operating point Analysis and Design, estimation of voltage gain, input resistance, output resistance for Single Stage Amplifier: CS stage with resistance load, Divide connected load, Current						

source load, Triode load, CS stage with source degeneration, Source follower, Common-gate stage, Cascade stage, Current Mirror.	
Differential Amplifiers	**[6 Hrs]**
Basic difference pair, Common mode response, Differential pair with MOS loads, Gilbert cell. Cascade current mirrors, Active current mirrors.	
Frequency response	**[6 Hrs]**
Fundamental concepts, Bode rules, Miller theorem, CS stage, Source follower, Common gate stage, Cascade stage and difference pair, Noise analysis	
Operational amplifiers design	**[6 Hrs]**
One stage OPAMP, two stage OPAMP, Gain boosting, Slew rate, PSRR. Design equations and procedure.	
Advanced OPAMP	**[6 Hrs]**
Cascode and folded cascode op-amps, common mode feedback techniques,Bandgap References, Introduction to Switched Capacitor Circuits, Nonlinearity and Mismatch.	

Textbooks:

[1]	Behzad Razavi, “Fundamentals of Microelectronics”, Wiley, 3rd edition, 2021.
[2]	Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, Mc Graw-Hill, 2nd edition, 2018

Reference Books:

[1]	Allen Holberg, “CMOS analog Circuit Design”,Oxford University Press, 3rd edition, 2017.
[2]	Donald Neamen, “Microelectronics Circuit Analysis and Design”, McGraw Hill, 4th Edition, 2021.
[3]	Jacob Millman, Christos C Halkias, Chetan D Parikh, “Integrated Electronics”, Mc Graw Hill Education, 2nd Edition, 2017

Note:

[1]	To measure CO1, questions may be of the type: explain modelling techniques and MOS characteristics.
[2]	To measure CO2, questions may involve design and analysis of amplifier circuits.
[3]	To measure CO3, questions may focus on OPAMP design and performance evaluation.
[4]	To measure SS, questions may include advanced analog circuit applications and design challenges.

Analog IC Design Lab						
Course Code	EVD-25005		**Examination Scheme**			
Teaching Scheme	3-0-2-1		**Theory**	TA: 20	MSE: 30	ESE: 50
Credits	4		**Laboratory**	ISE : 50	ESE:50	--

Course Outcomes: Students will be able to:

1. Interpret MOS transistor behavior using SPICE tools.
2. Perform DC, AC, noise, and frequency analysis of analog circuits.
3. Solve analog design problems using Cadence Virtuoso by modifying design parameters.

List of Practical:

1. DC analysis of NMOS and PMOS transistors using NGSPICE (estimate gm, gds).
2. AC analysis of NMOS and PMOS transistors using NGSPICE.
3. AC analysis of common source amplifier with different loads.
4. AC analysis of common gate and common drain amplifiers.
5. AC analysis of current source circuits.
6. DC and AC analysis of two-stage differential amplifier using Cadence.
7. Noise and frequency analysis of amplifiers using Cadence tools.
8. Design of bandgap reference circuits using Cadence.
9. Design of DAC using Cadence tools.
10. Design of ADC using Cadence tools.
11. Design of switched capacitor filters using Cadence.

Next Generation Computer Architectures						
Course Code	EVD(PE)-25001		**Examination Scheme**			
Teaching Scheme	3-0-0-1		Theory	TA: 20	MSE: 30	ESE: 50
Credits	3		Laboratory	ISE: 00	ESE: 00	--
Course Outcomes: Students will be able to:						
1. Understand and Analyze advanced processor architectures and performance metrics 2. Evaluate multi-core and parallel architectures 3. Apply concepts of GPU and heterogeneous computing 4. Analyze modern memory and storage systems 5. Compare domain-specific architectures 6. Explore emerging trends in next-generation computing systems						
Unit 1: Fundamentals of Advanced Computer Architecture						**[6 Hrs]**
Review of basic computer architecture concepts ,Instruction Set Architecture (ISA) ,evolution Performance metrics and benchmarking , Pipelining and superscalar architecture ,Instruction-level parallelism (ILP)						
Unit 2: Multi-Core and Many-Core Architectures						**[6 Hrs]**
Multi-core processors: design and challenges, Cache coherence protocols (MSI, MESI, MOESI) , Memory consistency models ,Interconnection networks (Bus, Mesh, NoC) ,Case study of modern processors						
Unit 3: Parallel Computing Architectures						**[8 Hrs]**
Thread-level parallelism (TLP), SIMD, MIMD architectures, GPU architecture and programming basics, Vector processors, VLIW Architecture, Parallel programming models (OpenMP, CUDA overview)						
Unit 4: Memory Systems and Storage Innovations						**[8 Hrs]**
Advanced cache design, Virtual memory enhancements, non-volatile memory (NVM, MRAM, PCM) ,3D memory and High Bandwidth Memory (HBM), Storage-class memory						
Unit 5: Domain-Specific and AI Architectures						**[8 Hrs]**
AI/ML accelerators (TPU, NPU) ,Tensor processing architectures, FPGA-based acceleration, Edge AI hardware, Neuromorphic computing basics						
Self-Study (SS): Emerging Trends in Computer Architecture						**[8 Hrs]**

Quantum computing basics, Approximate computing, Reconfigurable computing , Green computing and energy-efficient architectures, Security in modern processors

Textbooks:	
[1]	Computer Architecture: A Quantitative Approach, John L. Hennessy and David A. Patterson, 6th Edition, Morgan Kaufmann (Elsevier), 2019, ISBN: 978-0128119051
[2]	Structured Computer Organization, Andrew S. Tanenbaum and Todd Austin, 6th Edition, Pearson, 2013, ISBN: 978-0132916528
Reference Books:	
[1]	Computer Organization and Design RISC-V Edition, David A. Patterson and John L. Hennessy, 2nd Edition, Morgan Kaufmann, 2020, ISBN: 978-0128203316
[2]	Parallel Computer Architecture, David Culler, Jaswinder Pal Singh, Anoop Gupta, Morgan Kaufmann, 1999, ISBN: 978-1558603436
[3]	GPU Computing Gems Emerald Edition, Wen-mei W. Hwu, Morgan Kaufmann, 2011, ISBN: 978-0123849885
[4]	Domain-Specific Architectures, John L. Hennessy and David A. Patterson, 1st Edition, Morgan Kaufmann, 2018, ISBN: 978-0128203316.
Note:	
[1] [2] [3] [4] [5] [6]	To measure CO1, questions may be of the type: explain, analyze, and compare architectural concepts. To measure CO2, questions may involve evaluation of multi-core and parallel systems. To measure CO3, questions may focus on GPU and heterogeneous computing applications. To measure CO4, questions may include memory and storage system analysis. To measure CO5, questions may involve comparison of domain-specific architectures. To measure CO6, questions may be based on emerging trends and modern computing paradigms.

Machine Learning						
Course Code	EVD(PE)-25002		**Examination Scheme**			
Teaching Scheme	3-0-0-1		Theory	TA: 20	MSE: 30	ESE: 50
Credits	3		Laboratory	ISE: 00	ESE: 00	--

Course Outcomes: Students will be able to:

1. Understand popular machine learning algorithms along with their mathematical foundations.
2. Analyze the role of data in solving real-world problems using machine learning techniques.
3. Implement basic machine learning algorithms using standard libraries in Python

Introduction to Machine Learning	**[6 Hrs]**
Role of machine learning in computer science and problem solving. Features and data representation. Linear transformations and matrix-vector operations in the context of data. Classification and regression. Probability distributions and Bayes rule. Supervised and unsupervised learning.	
Fundamentals of Machine Learning	**[6 Hrs]**
Principal Component Analysis (PCA) and dimensionality reduction. Nearest Neighbors and KNN algorithm. Linear regression. Decision tree classifiers. Concept of generalization and overfitting. Training, validation, and testing methodologies.	
Core Machine Learning Algorithms	**[6 Hrs]**

Ensemble learning and Random Forests. Linear Support Vector Machines (SVM). K-Means clustering. Logistic regression. Naive Bayes classification.	
Neural Network Learning	**[6 Hrs]**
Loss functions and optimization techniques. Gradient descent and perceptron/delta learning rule. Multi-layer perceptron (MLP). Backpropagation algorithm. MLP for classification and regression. Regularization techniques.	
Deep Learning Fundamentals	**[6 Hrs]**
Introduction to deep learning. Convolutional Neural Networks (CNNs) and their applications. Overview of modern deep learning architectures.	
Self-Study (SS): Advanced Machine Learning Applications	**[4 Hrs]**
Applications of machine learning in real-world domains such as computer vision, natural language processing, and data analytics. Overview of recent trends and tools in machine learning.	

Textbooks:

[1]	Tom M. Mitchell, *Machine Learning*, McGraw Hill Education, International Edition
[2]	Christopher M. Bishop, *Pattern Recognition and Machine Learning*, 2nd Edition, Springer.

Reference Books:

[1]	Kevin P. Murphy, *Machine Learning: A Probabilistic Perspective*, MIT Press.
[2]	Ian Goodfellow, Yoshua Bengio, Aaron Courville, *Deep Learning*, MIT Press.

Note:

[1]	To measure CO1, questions may be of the type: explain algorithms and mathematical foundations.
[2]	To measure CO2, questions may involve data-driven problem solving and analysis.
[3]	To measure CO3, questions may be based on implementation and coding of ML algorithms.
[4]	To measure SS, questions may include application-based and case-study problems.

SoC architecture

Course Code	EVD(PE)-25003		**Examination Scheme**			
Teaching Scheme	3-0-0-1		Theory	TA: 20	MSE: 30	ESE: 50
Credits	3		Laboratory	ISE: 00	ESE: 00	--

Course Outcomes: Students will be able to:

1. Analyze and Integrate SoC Architectures and Protocols
2. Design, Implement, and Verify Systems at Multiple Levels
3. Manage HW-SW Co-design and System Security

Introduction to SoC	**[6 Hrs]**
Trends in computer systems. Definition of System-on-Chip (SoC), benefits, and design challenges.	
SoC Components and Interconnects	**[6 Hrs]**
Processing units including CPUs, accelerators, and IP cores. Memory systems and peripherals. On-chip interconnect architectures.	
SoC Implementation (ASIC and FPGA)	**[6 Hrs]**
Overview of VLSI design. FPGA architecture and implementation using Xilinx/Intel platforms.	
OS and Software Integration	**[6 Hrs]**
Operating system basics, resource management, and multithreading. Linux installation and configuration on FPGA-based SoC platforms.	
System-Level Design and Verification	**[6 Hrs]**

Models of computation. SystemC overview. Transaction-Level Modeling (TLM) including initiators and transactors. Verification techniques, verification flow, and tools such as UVM and SCV. Case studies.

Self-Study (SS): Security and Advanced SoC Concepts	**[6 Hrs]**
Hardware-software co-design for security. Hardware security fundamentals, IP protection, encryption techniques. Overview of memory systems and bus protocols including UART, I2C, AXI/AHB, AMBA, and PCI.	
Textbooks:	
[1]	David A. Patterson and John L. Hennessy, *Computer Organization and Design: The Hardware/Software Interface (ARM Edition)*.
[2]	Thorsten Grötker, Stan Krolikoski, Grant Martin, *System Design with SystemC*.
Reference Books:	
[1]	Pong P. Chu, *FPGA Prototyping by Verilog Examples (Xilinx Spartan/Artix editions)*.
[2]	Swarup Bhunia and Mark Tehranipoor, *Hardware Security: A Hands-On Learning Approach*.
Note:	
[1]	To measure CO1, questions may be of the type: explain SoC architecture and protocol integration.
[2]	To measure CO2, questions may involve system design, implementation, and verification.
[3]	To measure CO3, questions may focus on HW-SW co-design and system security.
[4]	To measure SS, questions may include advanced SoC concepts and protocol-based design scenarios.

Research Methodology

Course Code	SET-25001		**Examination Scheme**			
Teaching Scheme	2-0-0-1		Theory	TA: 20	MSE: 30	ESE: 50
Credits	3		Laboratory	ISE: 00	ESE: 00	--

Course Outcomes: Students will be able to:

1. Formulate research problems by defining objectives, hypotheses, variables, and feasibility.
2. Synthesize literature using reproducible search and screening strategies.
3. Apply research ethics, authorship norms, compliance rules, and FAIR data practices.
4. Produce research outputs through ethical analysis, documentation, and dissemination.

Introduction to Research	**[4 Hrs]**
What is scientific research, objectives of research, motivation, types of research, research approaches, research methodology, significance of research, indications of good research	
Designing a Problem:	**[6 Hrs]**
Research problems, literature review, formulation of feasible problem, hypothesis, errors in problem selection, selection of variables,	
Methods- Simulations and Experiments:	**[7 Hrs]**
Conventional approaches, selection of tools, setting up production, validation of results,	

performance analysis, sensitivity analysis, errors in measurements	
Statistics and Uncertainty Quantification:	**[7 Hrs]**
Data, importance of analyzing data, types of analyses, selection practices, statistics, sampling techniques, uncertainty quantification, errors analysis	
RCR and Ethics	**[5 Hrs]**
Responsible conduct of research, IEC compliance, what is plagiarism, QRPs, generative A.I. in research	
IPR, Research Ethics and Publishing:	**[8 Hrs]**
Introduction to IPR, significance of IPR, types of IPR, recent developments, technical writing	

Textbooks:

[1]	Melville, S., & Goddard, W. (1996). Research methodology: An introduction for science & engineering students. Juta & Co.
[2]	Kothari, C. R. (2009). Research methodology: Methods and trends. New Age International Publishers.

Reference Books:

[1]	Goddard, W., & Melville, S. (2001). Research methodology: An introduction (2nd ed.). Juta Academic.
[2]	Kumar, R. (2005). Research methodology: A step-by-step guide for beginners (2nd ed.). Sage Publications.
[3]	Sharma, S. D. (2001). Operational research. Kedar Nath Ram Nath & Co.

Note:

[1]	To measure CO1, questions may be of the type: define, identify, and formulate research problems.
[2]	To measure CO2, questions may involve literature review and synthesis methods.
[3]	To measure CO3, questions may focus on ethics, plagiarism, and compliance practices.
[4]	To measure CO4, questions may include documentation, analysis, and research dissemination.

Semester II

Verification using SV and UVM						
Course Code	EVD-25006		**Examination Scheme**			
Teaching Scheme	3-0-2-1		Theory	TA: 20	MSE: 30	ESE: 50
Credits	4		Laboratory	ISE: 50	ESE: 50	--

Course Outcomes: Students will be able to:

1. Develop reusable and layered testbench architectures.
2. Implement constrained-random verification and assertions.
3. Analyze verification progress using coverage metrics

Verification Fundamentals	**[6 Hrs]**
Verification guidelines including basic testbench functionality, directed testing, verification process, testbench components, constrained-random stimulus, functional coverage, layered testbench architecture, simulation phases, code reuse, and testbench performance.	
System Verilog Constructs	**[6 Hrs]**
Primitive testbench methodology, importance of verification, verification planning, System Verilog constructs and features.	
Data Types and Procedural Blocks	**[6 Hrs]**
Built-in data types, fixed-size arrays, dynamic arrays, queues, associative arrays, and array methods. Procedural blocks including fork-join, tasks, and functions.	
Inter process Communication and Interfaces	**[6 Hrs]**
Semaphore and mailbox mechanisms. Interfaces including ports, clocking blocks, virtual interfaces, and top-level program-module interactions.	
Advanced Verification Techniques	**[6 Hrs]**
Object-oriented programming concepts: inheritance and polymorphism. Randomization and constrained random techniques including pre-randomize and post-randomize. Code and functional coverage: cover groups, cover points, bins. System Verilog assertions including properties and Boolean expressions.	
Self-Study (SS): UVM Methodology	**[4 Hrs]**
Introduction to Universal Verification Methodology (UVM), reusable verification components, layered architecture, and real-world verification environments.	

Textbooks:

[1]	Chris Spears, *System Verilog for Verification*, 2nd Edition, Springer.
[2]	Janick Bergeron, *Writing Testbenches: Functional Verification of HDL Models*, Kluwer Academic Publishers.

Reference Books:

[1]	IEEE 1800-2009 Standard for SystemVerilog
[2]	SystemVerilog Official Website – www.systemverilog.org
[3]	Verification Academy (OVM/UVM Resources) – www.verificationacademy.com

Note:

[1]	To measure CO1, questions may be of the type: design and explain testbench architectures.
[2]	To measure CO2, questions may involve constrained-random verification and assertions.
[3]	To measure CO3, questions may focus on coverage metrics and verification analysis.

[4]	To measure SS, questions may include UVM-based verification scenarios and applications.

VLSI Physical Design						
Course Code	EVD-25006		**Examination Scheme**			
Teaching Scheme	3-0-2-1		Theory	TA: 20	MSE: 30	ESE: 50
Credits	3		Laboratory	ISE: 50	ESE: 50	--

Course Outcomes: Students will be able to:

Course Outcomes: At the end of the course, students will demonstrate the ability to

1. Understand the concepts of Physical Design Process such as partitioning; Floor planning, Placement and Routing.
2. Discuss the concepts of design optimization algorithms and their application to physical design automation.
3. Understand the concepts of simulation and synthesis in VLSI Design Automation
4. Formulate CAD design problems using algorithmic methods

Introduction to VLSI Design Automation	**[4 Hrs]**
Overview of VLSI design automation tools, algorithms, Structural and logic design. Transistor-level design, layout design, verification methods, and design management tools.	
Algorithmic graph theory and computational complexity	**[6 hrs]**
Data structures for representation of graphs, Computational complexity, Graph terminology, standard ways to represent graphs, Line graph, rectangular graph, graph search algorithms, BFS, DFS, Dijkstra shortest path algorithm, Minimum spanning tree,	
Partitioning and Floor Planning	**[6 Hrs]**
Floor planning concepts Layout compaction, difference between floor planning and placement, Design rules and symbolic layout. KL and FM portioning algorithm, files required for floor planning, optimization in floor planning, algorithms for floor planning : slicing floor plan, cluster growth, linear ordering algorithm	
Placement, CTS and Routing	**[8 Hrs]**
Standard cell placement, Global placement, Detailed Placement, Placement optimization, Power planning, algorithms like partition based, simulated annealing, force directed, congestion driven, Clock tree concepts: Clock buffering, clock tree topologies, CTS optimization techniques, HFNS Routing: Metal layer tracks, lower vs upper metal layer, Local routing, channel routing, global routing, and associated algorithms. PVT corners	
Signal integrity and Timing closure	**[6 Hrs]**
Reasons affecting signal integrity, cross talk and protection techniques, SDC constraints, PVT corners, MCMM	
Physical verification and tapeout	**[4 Hrs]**
DRC, LVS, ERC, Parasitic extraction, Antenna rule check, Electro migration, Physical Verification at Advanced Nodes	
Self-Study (SS): Advanced CAD and Optimization Techniques	**[4 Hrs]**
Advanced topics in CAD for VLSI, optimization techniques, and modern trends in physical design automation.	
Textbooks:	

[1]	S. H. Gerez, *Algorithms for VLSI Design Automation*, John Wiley (India), 2006.
[2]	N. A. Sherwani, *Algorithms for VLSI Physical Design Automation*, Kluwer, 2012.
Reference Books:	
[1]	S. M. Sait and H. Youssef, *VLSI Physical Design Automation*, Cambridge India, 2010.
[2]	M. Sarrafzadeh, *Introduction to VLSI Physical Design*, McGraw Hill, 1996.
[3]	Giovanni De Micheli, *Synthesis and Optimization of Digital Circuits*, McGraw Hill, 2017.
Note:	
[1] [2] [3] [4]	To measure CO1, questions may be of the type: explain physical design processes and concepts. To measure CO2, questions may involve analysis of optimization algorithms. To measure CO3, questions may focus on simulation and synthesis techniques. To measure CO4, questions may involve formulation and solution of CAD design problems.

VLSI Physical Design Lab						
Course Code	EVD-25007		**Examination Scheme**			
Teaching Scheme	3-0-2-1		**Theory**	TA: 20	MSE: 30	ESE: 50
Credits	4		**Laboratory**	ISE : 50	ESE:50	--

Course Outcomes: Students will be able to:

1. Apply constraints of VLSI fabrication technology to design automation tools using graph algorithms.
2. Simulate partitioning algorithms such as Kernighan–Lin and simulated annealing.
3. Optimize floor planning using time-driven and hierarchical methods.
4. Optimize routing using two-terminal and multi-terminal algorithms.

List of Practical:

Graph Algorithms
Graph search algorithms: Depth First Search (DFS), Breadth First Search (BFS). Spanning tree algorithms including Kruskal's algorithm. Shortest path algorithms: Dijkstra and Floyd–Warshall. Steiner tree algorithms.

Computational Geometry Algorithms
Line sweep method and extended line sweep method for geometric problem solving in VLSI design.

Partitioning Algorithms
Group migration algorithms: Kernighan–Lin algorithm and its extensions such as Fiduccia–Mattheyses and Goldberg–Burstein algorithms. Simulated annealing and simulated evolution algorithms. Metric allocation methods.

Floor Planning Algorithms
Constraint-based methods, integer programming approaches, rectangular dualization techniques, hierarchical tree-based methods, simulated evolution algorithms, and time-driven floor planning algorithms.

Routing Algorithms
Two-terminal routing: maze routing (Lee's, Soukup's, Hadlock algorithms), line-probe algorithm, shortest path-based routing. Multi-terminal routing: Steiner tree-based methods including SMST and Z-RST algorithms.

Textbooks:

1. Naveed Shervani, *Algorithms for Physical Design Automation*, 3rd Edition, Kluwer

Academic, 1998 **2.** Charles J. Alpert, Dinesh P. Mehta, Sachin S. Sapatnekar, *Handbook of Algorithms for Physical Design Automation*, CRC Press, 2008.

RF Circuit Design						
Course Code	EVD-25008		**Examination Scheme**			
Teaching Scheme	3-0-2-1		Theory	TA: 20	MSE: 30	ESE: 50
Credits	4		Laboratory	ISE: 50	ESE: 50	--

Course Outcomes: Students will be able to:

1. Understand RF system design fundamentals and analyze high-frequency amplifier design.
2. Evaluate low noise amplifier (LNA) topologies and design techniques.
3. Understand RF mixer requirements, operation, and performance parameters.
4. Analyze synthesizers, oscillators, and their characteristics.
5. Evaluate RF power amplifiers and effects of nonlinearities.

Overview of RF Systems	**[6 Hrs]**
Wireless transmitter and receiver architectures: heterodyne and superheterodyne systems. Basic RF design concepts, units, and time variance. Effects of nonlinearity: harmonic distortion, gain compression, cross modulation, intermodulation, cascaded nonlinear stages, AM/PM conversion. RF behavior of passive components: interconnects, resistors, capacitors, inductors, transformers, and transmission lines. Noise analysis: classical two-port noise theory and representation.	
High Frequency Amplifier Design	**[6 Hrs]**
Types of amplifiers: narrowband and wideband. Bandwidth enhancement using zeros. Shunt-series amplifiers, fT doublers, neutralization, and uni lateralization techniques	
Low Noise Amplifiers	**[6 Hrs]**
Need for LNA, Friis' equation. LNA design techniques and topologies including noise cancelling and distortion cancelling methods. Linearity and large-signal performance.	
RF Mixers and Frequency Synthesis	**[6 Hrs]**
Need for mixers and noise-linearity trade-offs. Mixer types: multiplier-based, subsampling, diode-ring mixers. Noise folding, single-sideband and double-sideband noise figure. Feedthrough in single-balanced and double-balanced mixers. IP2 and IP3 improvement. Oscillators and synthesizers: resonators, negative resistance oscillators, phase noise, and frequency synthesis techniques.	
RF Power Amplifiers and Layout	**[6 Hrs]**
Classes of RF power amplifiers: Class A, AB, B, C, D, E, and F. Power amplifier modulation and linearity considerations. RFIC	
Self-Study (SS): Advanced RF Design Techniques	**[4 Hrs]**
Advanced RFIC design challenges, emerging RF technologies, and practical considerations in high-frequency circuit implementation.	
Textbooks:	

[1]	Thomas H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd Edition, Cambridge University Press, 2004.
[2]	Behzad Razavi, *RF Microelectronics*, 2nd Edition, Prentice Hall, 1998.
Reference Books:	
[1]	A. Abidi, P. R. Gray, R. G. Meyer (Eds.), *Integrated Circuits for Wireless Communications*, IEEE Press, 1999.
[2]	R. Ludwig and P. Bretchko, *RF Circuit Design: Theory and Applications*, Pearson, 2000.
[3]	A. Mattuck, *Introduction to Analysis*, Prentice-Hall, 1998.
Note:	
[1] [2] [3] [4] [5]	To measure CO1, questions may be of the type: explain RF system concepts and amplifier design. To measure CO2, questions may involve LNA design and analysis. To measure CO3, questions may focus on mixer design and performance evaluation. To measure CO4, questions may include oscillator and synthesizer analysis. To measure CO5, questions may involve power amplifier design and nonlinear effects.

RF Circuit Design Lab						
Course Code	EVD-25008		**Examination Scheme**			
Teaching Scheme	3-0-2-1		**Theory**	TA: 20	MSE: 30	ESE: 50
Credits	4		**Laboratory**	ISE : 50	ESE:50	--
Course Outcomes: Students will be able to:						
1. Analyze RF circuits and components using simulation tools. 2. Design and evaluate amplifiers, mixers, and oscillators at high frequencies. 3. Perform RF measurements and interpret results for performance parameters such as gain, noise, and linearity						
List of Practical:						
1. Simulation of basic RF components (resistors, capacitors, inductors, transmission lines) at high frequencies. 2. Design and analysis of narrowband and wideband RF amplifiers. 3. Simulation and performance evaluation of Low Noise Amplifier (LNA). 4. Analysis of RF mixer circuits and study of conversion gain and linearity. 5. Design and simulation of oscillators and frequency synthesizers. 6. Noise analysis in RF circuits using simulation tools. 7. Design and analysis of RF power amplifiers (Class A, B, AB). 8. Study of nonlinearity effects such as harmonic distortion and intermodulation. 9. RF circuit layout and parasitic analysis using CAD tools. **10.** Case study-based RF system design and simulation.						

VLSI Testing						
Course Code	EVD(PE)-25005		**Examination Scheme**			
Teaching Scheme	3-0-0-1		Theory	TA: 20	MSE: 30	ESE: 50
Credits	3		Laboratory	ISE: 00	ESE: 00	--

Course Outcomes: Students will be able to:

1. Understand testing concepts, fault models, and testing methodologies in VLSI systems.
2. Apply test pattern generation techniques and algorithms for digital circuits.
3. Analyze design-for-testability (DFT) and built-in self-test (BIST) techniques.

Introduction to Testing	**[6 Hrs]**
Testing philosophy, role of testing in VLSI design, types of testing, test economics, yield concepts, rule of 10, and Automatic Test Equipment (ATE).	
Fault Modelling	**[6 Hrs]**
Defects, errors, and faults. Fault modeling techniques including stuck-at faults, bridging faults, state-dependent faults, multiple faults, and fault collapsing.	
Test Pattern Generation	**[6 Hrs]**
Test generation techniques: Boolean difference, path sensitization, SCOAP (controllability and observability), random test generation, and D-algorithm.	
Design for Testability (DFT)	**[6 Hrs]**
Concept of making circuits testable. Scan design techniques, testability insertion, and associated overheads.	
Built-In Self-Test (BIST)	**[6 Hrs]**
BIST concepts and techniques. Boundary scan architecture and testing methodologies.	
Self-Study (SS): Advanced Testing Techniques	**[4 Hrs]**
Advanced topics in VLSI testing, modern testing challenges, and emerging trends in test automation.	

Textbooks:

[1]	Zainalabedin Navabi, *Digital System Test and Testable Design Using HDL Models and Architectures*, Springer.
[2]	Michael L. Bushnell and Vishwani D. Agrawal, *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits*, Kluwer Academic Publishers.

Reference Books:

[1]	P. K. Lala, *Digital Circuit Testing and Testability*, Academic Press
[2]	M. Abramovici, M. A. Breuer, A. D. Friedman, *Digital Systems Testing and Testable Design*, IEEE Press.

Note:

[1]	To measure CO1, questions may be of the type: explain testing concepts and fault models
[2]	To measure CO2, questions may involve test pattern generation techniques and algorithms.
[3]	To measure CO3, questions may focus on DFT and BIST techniques.

VLSI architectures for Signal Processing						
Course Code	EVD(PE)-25006		**Examination Scheme**			
Teaching Scheme	3-0-0-1		Theory	TA: 20	MSE: 30	ESE: 50
Credits	3		Laboratory	ISE: 00	ESE: 00	--

Course Outcomes: Students will be able to:

1. Understand DSP system architectures and their implementation in VLSI.

2. Analyze data flow graphs and compute iteration bounds for DSP systems.
3. Apply pipelining and parallel processing techniques for performance and power optimization.
4. Design efficient architectures using unfolding and folding transformations.
5. Analyze architectures for recursive, adaptive filters, and DSP processors.

Introduction to DSP Systems	**[6 Hrs]**
Introduction to digital signal processing systems. Typical DSP algorithms. Application demands of DSP systems and impact of scaled technologies	
Iteration Bound and Data Flow Graphs	**[6 Hrs]**
Data flow graph representation. Loop bound and iteration bound concepts. Iteration bound computation for multi rate data flow graphs.	
Pipelining and Parallel Processing	**[6 Hrs]**
Pipelining of FIR filters. Parallel processing techniques. Combined pipelining and parallel processing for performance improvement and low-power design.	
Unfolding and Folding Transformations	**[6 Hrs]**
Unfolding algorithms and properties. Applications of unfolding. Folding transformation and register minimization in folded architectures.	
Recursive and Adaptive Filter Architectures	**[6 Hrs]**
Pipelining in IIR filters. Parallel processing for IIR filters. Pipelined adaptive digital filters. Overview of programmable DSP processors and their features for mobile and wireless applications.	
Self-Study (SS): Advanced DSP Architectures	**[8 Hrs]**
Advanced VLSI architectures for DSP applications, emerging trends in signal processing hardware, and optimization techniques.	

Textbooks:

[1]	Keshab K. Parhi, *VLSI Digital Signal Processing Systems: Design and Implementation*, Wiley.

Reference Books:

[1]	S. Y. Kung, H. J. Whitehouse, T. Kailath, *VLSI and Modern Signal Processing*, Prentice Hall.
[2]	L. R. Rabiner and B. Gold, *Theory and Application of Digital Signal Processing*, Prentice Hall.

Note:

[1]	To measure CO1, questions may be of the type: explain DSP architectures and applications.
[2]	To measure CO2, questions may involve data flow graphs and iteration bound calculations.
[3]	To measure CO3, questions may focus on pipelining and parallel processing techniques.
[4]	To measure CO4, questions may involve unfolding and folding transformations.
[5]	To measure CO5, questions may include analysis of filter architectures and DSP processor

Hardware / Software Co-design

Course Code	EVD(PE)-25007		**Examination Scheme**			
Teaching Scheme	3-0-0-1		Theory	TA: 20	MSE: 30	ESE: 50
Credits	3		Laboratory	CIE: 00	ESE: 00	--

Course Outcomes: Students will be able to:

1. Design and Implement Hardware Cryptographic Co-processors
2. Evaluate Vulnerabilities to Physical and Micro-architectural Attacks
3. Implement Secure Design-for-Testability (DfT) and Robust Protection

Introduction to hardware Cryptography:	**[6 Hrs]**
Finite fields and their role in cryptography. AES hardware implementation and S-Box design. Mapping cryptographic algorithms to hardware. Introduction to elliptic curve cryptography (ECC) and hardware implementation of ECC.	
Introduction to Side Channel Analysis	**[6 Hrs]**
Introduction to side-channel attacks. Advanced side-channel analysis techniques. Power analysis and timing attacks. Introduction to fault attacks.	
Types of crypto processor	**[6 Hrs]**
Advanced fault attack techniques including algebraic fault analysis. Detection and mitigation strategies for fault attacks in hardware systems.	
Cryptographic Processor Architectures	**[6 Hrs]**
Types of cryptographic processors: tamper-resistant processors, homomorphic cryptoprocessors, open-source cryptographic processors, and reconfigurable cryptographic processors.	
Self-Study (SS): Emerging Trends in Hardware Security	**[4 Hrs]**
Emerging threats and defenses in hardware security. Secure hardware design practices and future directions in cryptographic hardware.	

Textbooks:	
[1]	M. Tehranipoor and C. Wang, *Introduction to Hardware Security and Trust*, Springer.
[2]	Debdeep Mukhopadhyay and Rajat Subhra Chakraborty, *Hardware Security: Design, Threats, and Safeguards*, CRC Press.
Reference Books:	
[1]	Tom St. Denis, *Cryptography for Developers*, Syngress.
Note:	
[1]	To measure CO1, questions may be of the type: explain and design cryptographic hardware systems.
[2]	To measure CO2, questions may involve analysis of side-channel and fault attacks.
[3]	To measure CO3, questions may focus on secure design techniques and DFT methods.

Mixed Signal Circuit Design						
Course Code	EVD(PE)-25008		**Examination Scheme**			
Teaching Scheme	3-0-0-1		Theory	TA: 20	MSE: 30	ESE: 50
Credits	3		Laboratory	CIE: 00	ESE: 00	--

Course Outcomes: Students will be able to:

1. Design and optimize mixed-signal building blocks.
2. Analyze and characterize data converters.
3. Model and implement clock generation systems.

Fundamentals of Mixed-Signal Design & Basic Building Blocks	**[6 Hrs]**
Concepts of mixed-signal design and performance measures. Design methodology using the The \$g_m/I_D\$ approach. Basic building blocks including current mirrors and voltage references.	

Operational amplifier design and analysis for mixed-signal environments.	
Comparators and Switched-Capacitor Circuits	**[6 Hrs]**
Comparator design and characterization: two-stage and open-loop comparators. CMOS digital circuits and MOSFET switch design. Switched-capacitor (SC) circuits: principles and layout considerations. Sample-and-hold (S/H) circuits: architectures and limitations.	
Data Converters – Principles and Nyquist Rate	**[6 Hrs]**
Introduction to ADCs and DACs. Performance metrics such as DNL, INL, SNR, and SFDR. Nyquist-rate DAC architectures. Nyquist-rate ADCs including Flash, SAR, pipelined, and time-interleaved ADCs. Continuous-time filter design with frequency and Q tuning.	
Phase-Locked Loops (PLL) & Frequency Synthesis	**[6 Hrs]**
PLL architecture: VCO, dividers, phase detectors, and loop filters. PLL analysis: lock behaviour, linearized small-signal models, second-order PLL models, and limitations. Practical PLL design and characterization.	
Oversampling Converters, Jitter, and Phase Noise	**[6 Hrs]**
Oversampling (Sigma-Delta) ADCs. Jitter analysis including period, cycle-to-cycle, and spectral representations. Oscillator noise: ring and LC oscillators, phase noise. Impact of jitter and phase noise in PLL systems. Design of frequency and Q tunable continuous-time filters.	
Self-Study (SS): Advanced Mixed-Signal Systems	**[4 Hrs]**
Advanced mixed-signal IC design challenges, system-level integration, and emerging applications in communication and signal processing.	

Textbooks:	
[1]	Behzad Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd Edition.
[2]	R. J. Baker, *CMOS Mixed-Signal Circuit Design*, 2nd Edition, Wiley-IEEE Press, 2008.
Reference Books:	
[1]	Allen and Holberg, *CMOS Analog Circuit Design*.
[2]	Behzad Razavi, *Principles of Data Conversion System Design*, Wiley-IEEE Press, 1994.
[3]	Vineeta P. Gejji, *Analog and Mixed Mode VLSI Design*, PHI Learning.
[4]	M. Gustavsson, J. J. Wikner, N. N. Tan, *CMOS Data Conversion for Communications*, Springer, 2000.
Note:	
[1] [2] [3]	To measure CO1, questions may be of the type: design and analyze mixed-signal building blocks. To measure CO2, questions may involve data converter architectures and performance evaluation. To measure CO3, questions may focus on PLL design and clock generation systems.

Advanced VLSI Design						
Course Code	EVD(PE)-25009		**Examination Scheme**			
Teaching Scheme	3-0-0-1		Theory	TA: 20	MSE: 30	ESE: 50
Credits	3		Laboratory	CIE: 00	ESE: 00	--

Course Outcomes: Students will be able to:

1. Analyse Power Dissipation & Scaling Impacts
2. Design Low-Power Memory & Logic Architectures
3. Model Interconnect Parasitic & Testability

Low Power Design Techniques	**[6 Hrs]**
Components of power dissipation in CMOS circuits. Threshold voltage scaling and its effects. Impact of scaling on dynamic power. Circuit topologies for low-power design. Leakage power contributors and mitigation techniques. Low-power design methodologies including Dynamic Voltage and Frequency Scaling (DVFS), pipelining, and parallel processing.	
Low Power Memory Design	**[6 Hrs]**
Transistor scaling and leakage mechanisms. Leakage control techniques at circuit level. Methods such as MTCMOS, SCCMOS, VTCMOS, and DTMOS. Cache memory leakage issues. Noise margin considerations. Parametric failures in SRAM and leakage reduction schemes. Supply gating techniques.	
Testability and Power-Aware Testing	**[6 Hrs]**
IDDQ testing, stuck-at fault testing, test power issues, test coverage enhancement, and gated decoupling capacitance techniques.	
Interconnect Modeling	**[6 Hrs]**
Capacitive, resistive, and inductive parasitics. Electrical wire modeling as transmission lines. Impact of interconnect on performance. Advanced interconnect techniques for high-speed VLSI design.	
Advanced Optimization Techniques	**[6 Hrs]**
Integration of low-power, high-performance design strategies. Trade-offs between power, performance, and area. Emerging techniques in advanced VLSI design.	
Self-Study (SS): Emerging Trends in Low-Power VLSI	**[4 Hrs]**
Recent developments in low-power design, advanced memory technologies, and future challenges in VLSI scaling.	

Textbooks:

[1]	Kaushik Roy and Sharat Prasad, *Low Power CMOS VLSI Circuit Design*, John Wiley & Sons, 2000.
[2]	J. M. Rabaey, A. Chandrakasan, B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, Pearson.

Reference Books:

[1]	Neil H. E. Weste and David Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, Pearson.
[2]	Sung-Mo Kang and Yusuf Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, McGraw Hill.

Note:

[1]	To measure CO1, questions may be of the type: analyze power dissipation and scaling effects.
[2]	To measure CO2, questions may involve design of low-power memory and logic circuits
[3]	To measure CO3, questions may focus on interconnect modeling and testability techniques

Nano-electronic material and devices						
Course Code	EVD(PE)-25010		**Examination Scheme**			
Teaching Scheme	3-0-0-1		Theory	TA: 20	MSE: 30	ESE: 50
Credits	3		Laboratory	ISE: 00	ESE: 00	--

Course Outcomes: Students will be able to:

1. Analyze Scaling Limits and Transport Physics
2. Evaluate Advanced Gate Stacks and Channel Materials
3. Design and Compare Non-Classical Device Architectures

Scaling Theory and Physical Limits **[6 Hrs]**

Fundamentals: Technology node definition, MOS Capacitor physics, Moore’s Law vs. Koomey's Law.
Scaling Theory: MOS Scaling (Constant field vs. Constant voltage), Short Channel Effects (SCEs), and Drain Induced Barrier Lowering (DIBL).
Case Study: Detailed description of a typical 65 nm CMOS technology.
Nano-Characterization: Overview of Nano-devices, Nano-materials, and characterization techniques.

Gate Stack and Transport Physics **[6 Hrs]**

Dielectrics: SiO2 vs. High-k gate dielectrics, Integration issues, Interface states, and reliability (Qbd).
Metal Gate Technology: Motivation, workfunction requirements, and integration challenges.
Carrier Transport: Velocity saturation, Ballistic transport, injection velocity, and velocity overshoot in Nano-MOSFETs.
Measurement: Advanced CV and IV characterization techniques.

Non-Classical & Multi-Gate Transistors **[6 Hrs]**

SOI Technology: Partially Depleted (PDSOI) and Fully Depleted (FDSOI) architectures.
Multi-Gate Structures: Ultra-thin body SOI, Double-gate transistors, and integration hurdles.
Vertical Devices: FinFETs and Cylindrical Gate (GAA) FETs—architectures and advantages.

Alternative Channel Materials & Junctions **[6 Hrs]**

Advanced Materials: Germanium (Ge) Nano-MOSFETs; Advantages of Ge over Silicon, strain engineering, and quantization effects.
Compound Semiconductors: III-V MOSFETs, Heterostructure MOSFETs, and channel quantization.
Contacts: Metal Source/Drain junctions, Schottky junctions on Si/Ge, and the Workfunction Pinning effect.

Novel Devices and Emerging Nanomaterials **[5 Hrs]**

Steep Subthreshold Devices: Tunnel FET (TFET) and Negative-Capacitance FET (NCFET).
Carbon Nanostructures: Carbon Nanotubes (CNTs), Graphene, and Nanotube FETs.
Quantum Structures: Quantum dots, nanorods, and other low-dimensional nano-structures.

Self-Study (SS): Emerging Nanoelectronics Technologies **[8 Hrs]**

Recent advances in nanoelectronics, quantum devices, and future scaling challenges in semiconductor technology.

Textbooks:

[1]	Y. Taur and T. Ning, “Fundamentals of Modern VLSI devices” Cambridge University Press
[2]	J. P. Colinge, “FinFETs and Other Multi-Gate Transistors,” Springer. 2009
[3]	John H. Davies, “The Physics of Low-Dimensional Semiconductors”,

Reference Books:

[1]	N. Collaert, “High Mobility Materials for CMOS Applications”,

[2]	Supriyo Datta, Lessons from Nanoelectronics A new Prospective on transport – Part A: Basic Concepts, World Scientific, 2017.
[3]	Related research papers.
Note:	
[1] [2] [3]	To measure CO1, questions may be of the type: analyze scaling effects and transport mechanisms. To measure CO2, questions may involve evaluation of gate stacks and advanced materials. To measure CO3, questions may focus on design and comparison of novel device architectures.

Hardware Security						
Course Code	EVD(PE)-25011		**Examination Scheme**			
Teaching Scheme	3-0-0-1		Theory	TA: 20	MSE: 30	ESE: 50
Credits	3		Laboratory	CIE: 00	ESE: 00	--

Course Outcomes: Students will be able to:

1. Design and Implement Hardware Cryptographic Co-processors
2. Evaluate Vulnerabilities to Physical and Micro-architectural Attacks
3. Implement Secure Design-for-Testability (DfT) and Robust Protection

Introduction to hardware Cryptography	**[6 Hrs]**
Finite Fields, AES Hardware, S-Box, Algorithm to Hardware, Intro to ECC, Hardware Design of ECC	
Introduction to Side Channel Analysis:	**[6 Hrs]**
Advanced SCA, Introduction to Fault AttacksAdvanced Fault Attacks, Algebraic Fault Analysis Design-for-Testability for Cryptographic Designs, Introduction to Micro-architectural attacks	
Types of crypto processor	**[6 Hrs]**
Tamper resistance cryptographic processor, Homomorphic cryptoprocessor design, Open-source cryptographic processor, Reconfigurable cryptographic processor	
Self-Study (SS): Emerging Trends in Hardware Security	**[4 Hrs]**
Recent advancements in hardware security, secure processor design, and future challenges in cryptographic hardware.	

Textbooks:	
[1]	M. Tehranipoor and C. Wang, *Introduction to Hardware Security and Trust*, Springer.
[2]	Debdeep Mukhopadhyay and Rajat Subhra Chakraborty, *Hardware Security: Design, Threats, and Safeguards*, CRC Press.
Reference Books:	
[1]	Tom St. Denis, “Cryptography for developers”, Syngress
Note:	
[1] [2] [3]	To measure CO1, questions may be of the type: design and analyze cryptographic hardware. To measure CO2, questions may involve side-channel and fault attack analysis. To measure CO3, questions may focus on DfT and secure design techniques.

Device Modelling

Course Code	EVD(PE)-25012		**Examination Scheme**			
Teaching Scheme	3-0-0-1		Theory	TA: 20	MSE: 30	ESE: 50
Credits	3		Laboratory	CIE: 00	ESE: 00	--

Course Outcomes: Students will be able to:

1. Analyze MOS Electrostatics and Non-idealities
2. Model Multi-Carrier Device Physics
3. Evaluate Compact Modeling for Advanced Architectures

MOS Capacitor	**[6 Hrs]**

Energy band diagram of Metal-Oxide-Semiconductor contacts, Mode of Operations: Accumulation, Depletion, Midgap, and Inversion, 1D Electrostatics of MOS, Depletion Approximation, Accurate Solution of Poisson's Equation, CV characteristics of MOS, LFCV and HFCV, Non-idealities in MOS, oxide fixed charges, interfacial charges.

The MOS transistor	**[6 Hrs]**

Small signal modelling for low frequency and High frequency, Pao-Sah and Brews models; Short channel effects in MOS transistors.

The bipolar transistor	**[6 Hrs]**

Ebers-Moll model; charge control model; small-signal models for low and high frequency and switching characteristics

Compact Modelling	**[6 Hrs]**

Compact model Level 1, Level 2, Level 3, UTB/FD SOI MOSFET, FinFETs: I-V characteristics, device capacitances, parasitic effects of extension regions, performance of simple combinational gates and amplifiers, novel circuits using FinFETs and GAA devices.

Self-Study (SS): Emerging Device Models	**[4 Hrs]**

Advanced compact models, nanoscale device modeling, and future directions in semiconductor device simulation.

Textbooks:

[1]	S. M. Sze, Physics of Semiconductor Devices, (2e), Wiley Eastern, 1981.
[2]	M. Lundstrom, Fundamentals of Nanotransistors, World Scientific Publishing Co Pte Ltd 2017.

Reference Books:

[1]	Y. P. Tsividis, Operation and Modelling of the MOS Transistor, McGraw-Hill, 1987.
[2]	E. Takeda, Hot-carrier Effects in MOS Trasistors, Academic Press, 1995.
[3]	J. P. Colinge, "FinFETs and Other Multi-Gate Transistors," Springer. 2009

Note:

[1]	To measure CO1, questions may be of the type: analyze MOS capacitor behavior and non-idealities.
[2]	To measure CO2, questions may involve modeling of MOS and bipolar transistors.
[3]	To measure CO3, questions may focus on compact modeling and advanced device architectures.

Technical Communication Skills						
Course Code	SET-25002		**Examination Scheme**			
Teaching Scheme	1-0-2-1		Theory	TA: 20	MSE: 30	ESE: 50
Credits	2		Laboratory	ISE: 00	ESE: 00	--

Course Outcomes: Students will be able to:

1. Produce Industry-Standard Technical Documentation
2. Deliver Impactful Technical Presentations
3. Master Collaborative and Digital Communication

Fundamentals of Technical Writing	**[6 Hrs]**

The Communication Cycle: Audience analysis, purpose identification, and technical clarity.
Grammar & Style: Eliminating ambiguity, active vs. passive voice in engineering, and the "Plain English" movement.
Ethics: Plagiarism, intellectual property (IP) basics, and data integrity in reporting.

Professional Documentation	**[6 Hrs]**

Structural Elements: Creating abstracts, executive summaries, and tables of contents.
Specific Formats: Writing Standard Operating Procedures (SOPs), White Papers, and Research Proposals.
The VLSI Perspective: Drafting Design-for-Test (DFT) reports and Verification plans

Visual Communication & Data Visualization	**[6 Hrs]**

Graphic Design for Engineers: Effective use of tables, flowcharts, timing diagrams, and schematics.
Tools: Introduction to LaTeX for thesis writing and Draw.io/Visio for technical diagrams.
Data Presentation: Transforming raw simulation results (from SPICE/Matlab) into meaningful charts.

Oral Communication & Presentation Skills	**[6 Hrs]**

Presentation Design: The 10-20-30 rule, slide hierarchy, and managing cognitive load.
Public speaking: Handling Q&A sessions, body language, and voice modulation.
Virtual Presence: Best practices for technical meetings on Zoom/Teams/Webex.

Career & Collaborative Communication	**[6 Hrs]**

Professional Identity: Resume/CV building for VLSI roles, Cover letters, and LinkedIn profile optimization.
Team Dynamics: Collaborative writing using Git/GitHub and Overleaf.
Networking: Writing professional emails, cold-outreach for internships, and interview etiquette.

Textbooks:

[1]	Meenakshi Raman & Sangeeta Sharma, “Technical Communication: Principles and Practice”, Oxford University Press
[2]	M. Ashraf Rizvi, “Effective Technical Communication”, McGraw Hill

Reference Books:

[1]	Michael Alley, The Craft of Scientific Writing, Springer.
[2]	Strunk & White, The Elements of Style by
[3]	Robert E. Berger, A Scientific Approach to Writing for Engineers and Scientists, IEEE Press.

Note:

[1] To measure CO1, tasks may include technical report writing and documentation exercises.
[2] To measure CO2, evaluation may include presentations and viva sessions.
[3] To measure CO3, activities may include collaborative writing and professional

	communication tasks.

Technical Communication Skills Lab						
Course Code	SET-25002		**Examination Scheme**			
Teaching Scheme	1-0-2-1		Theory	TA: 20	MSE: 30	ESE: 50
Credits	2		Laboratory	ISE: 00	ESE: 00	--

Course Outcomes: Students will be able to:

1. Produce effective dialogue for business related situations
2. Use listening, speaking, reading and writing skills for communication purposes and attempt tasks by using functional grammar and vocabulary effectively
3. Analyze critically different concepts / principles of communication skills
4. Demonstrate productive skills and have a knack for structured conversations
5. Appreciate, analyze, evaluate business reports and research papers

List of Practical:

Fundamentals of Communication: 7 Cs of communication, common errors in English, enriching vocabulary, styles and registers

Aural-Oral Communication: The art of listening, stress and intonation, group discussion, oral presentation skills

Reading and Writing: Types of reading, effective writing, business correspondence, interpretation of technical reports and research papers